

REMARKS

Claims 1, 4, 18, 20, 22, 26 and 28-31 have been amended and claims 33-36 have been added. Claims 1-36 are pending in the application. Reconsideration of the application is requested in view of the amendments and the remarks to follow.

New claims 33-36 are supported at least by text appearing at p. 8, line 11 through p. 14, line 3 of the application as originally filed. No new matter is added by new claims 33-36. New claims 33-36 distinguish over the art of record and are allowable.

Claims 1, 4, 18, 20, 22, 26 and 28-31 have been amended to more clearly recite the claimed subject matter, however, these amendments are not intended to alter the scope of the claims.

Rejection Under 35 U.S.C. §102:

Claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30 and 32 stand rejected under 35 U.S.C. 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,088,780 to Yamada et al., (hereinafter "Yamada"). Applicant respectfully disagrees and requests reconsideration and allowance of the subject application.

Anticipation is a legal term of art. Applicant notes that in order to provide a valid finding of anticipation, several conditions must be met: (i) the reference must include every element of the claim within the four corners of the reference (see MPEP §2121); (ii) the elements must be set forth as they are recited in the claim (see MPEP §2131); (iii) the teachings of the reference cannot be modified (see MPEP §706.02, stating that "No question of obviousness is present" in conjunction with anticipation); and (iv) the reference must enable the invention as recited in the claim (see MPEP §2121.01). Additionally, (v) these conditions must be simultaneously satisfied.

The §102 rejection of claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30 and 32 is believed to be in error. Specifically, the PTO and Federal Circuit provide that §102 anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of this rule is that the absence from a cited §102 reference of any claimed element negates the anticipation. *Kloster Speedsteel AB, et al. v. Crucible, Inc., et al.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986).

No §103 rejection has been lodged regarding claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30 and 32. Accordingly, if Applicant can demonstrate

that Yamada does not disclose any one claimed element with respect to claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30 and 32, the §102 rejections must be withdrawn, and a subsequent non-final action made with a different rejection in the event that the Examiner still finds any of such claims to be not allowable.

Applicant notes the requirements of MPEP §2131, which states that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM." This MPEP section further states that "'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

Yamada relates to a (Title) "Page table walker that uses at least one of a default page size and a page size selected for a virtual address space to position a sliding field in a virtual address". Yamada teaches (Abstract) "A method and apparatus for implementing a page table walker that uses at least one of a default page size and a page size selected for a virtual address space to position a sliding field in a virtual address. According to one aspect of the invention, an apparatus for use in a computer system is provided that includes a page size storage area and

a page table walker. The page size storage area is used to store a number of page sizes each selected for translating a different set of virtual addresses. The page table walker includes a selection unit coupled to the page size storage area, as well as a page entry address generator coupled to the selection unit. For each of the virtual address received, the selection unit positions a field in that virtual address based on the page size selected for translating the set of virtual addresses to which that virtual address belongs. In response to receiving the bits in the field identified for each of the virtual addresses, the page entry address generator identifies an entry in a page table based on those bits."

Yamada (Field of the Invention) states that "More specifically, the invention relates to the area of memory management." Yamada further (Background; col. 1, line 24 et seq.) states that:

Memory addressing schemes often use a technique called paging to implement virtual memory. When using paging, the virtual address space (i.e., the address space generated by either the execution unit of a processor or by the execution unit in conjunction with a segmentation unit of a processor) is divided into fix sized blocks called pages, each of which can be mapped onto any of the physical addresses (i.e., the addresses that correspond to hardware memory locations) available on the system. In a typical computer system, a memory management unit determines and maintains, according to paging algorithm(s), the current mappings for the virtual to physical addresses using one or more page tables.

Upon receiving a virtual address from the execution unit of a processor, typical memory management units initially translate the virtual address into its corresponding physical address using the page table(s). Since the page table(s) are often stored in main memory, accessing the page tables is time consuming. To speed up the paging translations, certain computer systems store the most recently used translations in a translation look-aside buffer or TLB (a faster memory that is often located on the processor). Upon generating a virtual address requiring translation, the memory management unit first searches for the translation in the TLB before accessing the page table(s). If the translation is stored in the TLB, a TLB "hit" is said to have occurred and the TLB provides the translation.

However, if the translation is not stored in the TLB, a TLB "miss" is said to have occurred and a page table walker is invoked to access the page tables and provide the translation.

In contrast, claim 1 recites "In a computing device having a processor that generates a first address signal of a first width and one or more peripheral devices that are addressed with a second address signal of a second width that is greater than the first width, wherein the second address signal is produced in the computing device by concatenating an address extension from an address extension register with the first address signal, a method comprising: concurrently executing threads of a plurality of application programs, wherein different ones of the threads indicate one or more address extensions to an operating system; storing the address extensions for use by the operating system; repeatedly switching between execution of the threads; and prior to executing a particular thread, writing the address extension of the base address indicated by the particular thread to the extension register", which is not taught or disclosed by Yamada.

Yamada is silent with respect to any "one or more peripheral devices" as recited in claim 1. In fact, Yamada is void of the term "peripheral". Further, Yamada is silent with respect to addressing any peripheral device using a "second address signal of a second width that is greater than the first width", as recited in claim 1.

The various elements described by Yamada all relate to a memory addressing scheme and are completely unrelated to the subject matter of any of Applicant's claims. In fact, the Office Action states (p. 4, item 5) that "Yamada et al. did not clearly disclose a method as recited in claim 1, wherein individual address extensions identify address ranges associated with one or more peripheral

devices." As such, the Examiner has admitted, on the record, that Yamada does not anticipate the subject matter recited in independent claim 1.

Yamada is silent with respect to any "processor address signal that is combined with an extended address signal to create a peripheral address signal", as recited in independent claim 5. Yamada is also silent with respect to any "concatenating the address extension with the processor address signal to create a peripheral address signal used by the first execution thread", as recited in independent claim 8.

Yamada also is silent with respect to "one or more peripheral devices that are addressed with a second address signal of a second width that is greater than the first width", as recited in independent claim 12. Yamada as well fails to teach or disclose "one or more peripheral devices that are addressed with a second address signal having a second width that is greater than the first width; an address extension register that stores an address extension, wherein the address extension is combined with the first address signal to create the second address signal", as recited in independent claim 16. Yamada further does not teach or disclose "one or more peripheral devices that are addressed with a second address signal having a second width that is greater than the first width; an address extension register that stores an address extension, wherein the address extension is combined with the first address signal to create the second address signal", as recited in independent claim 20.

Yamada is silent with respect to a program including "instructions for performing read/write operations on a peripheral device, wherein loading an

extension register is a predicate to performing said read/write operations", as recited in independent claim 24.

Claim 26 recites "A computer program stored in a storage medium for execution on a computer, the computer program being configured to cause the computer to perform acts of: executing an interruptible execution thread of the program; writing an address extension value associated with the execution thread to an extension register and contemporaneously to a memory location; associating the memory location with the execution thread; retrieving the value associated with the execution thread from the memory location when execution of the execution thread is resumed after being interrupted; writing the value retrieved from the memory location to the extension register; and resuming application of the execution thread", which is not taught or disclosed by Yamada. In fact, Yamada is void of the term "interrupt" and thus cannot and does not provide any teaching relative to an uninterruptable execution thread, writing anything to an extension register or a memory location in execution of such a thread, or retrieving anything from memory after resuming execution of such a thread after being interrupted.

The portions of Yamada cited in the Office Action specifically describe addressing of virtual memory pages and are unrelated to the affirmatively-recited aspects of any of Applicant's independent claims. In fact, Yamada is void of the term "peripheral" and does not teach addressing anything other than memory.

The Office Action states (p. 3, 4) that various affirmatively-recited elements are "inherently" disclosed by Yamada. Applicant notes that guidelines for application of the doctrine of inherency is discussed in MPEP §2112, entitled

"Requirements of Rejection Based on Inherency; Burden of Proof". This MPEP section points out that inherency is a doctrine relating to results, characteristics or function, and, as such, this doctrine does not support inference of affirmatively-recited elements. Further, the burden is on the Examiner to establish that such result, characteristic or function is inherent in the teachings of the reference.

In a subsection entitled "EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY", this MPEP section states: "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993)." Accordingly, it is improper to simply assert, without demonstration, that some affirmatively-recited element or elements are "inherent" in the cited reference. For at least these reasons, the anticipation rejections are in error and should be withdrawn, and Applicant's claims should be allowed.

Dependent claims 2, 4, 6, 7, 10, 11, 15, 18, 19, 22, 23, 25, 28-30 and 22 distinguish by virtue of dependence from allowable claims and for their own recited features that are neither taught nor disclosed by the cited reference. For at least these reasons, the anticipation rejection of claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30 and 32 should be withdrawn, and claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30 and 32 should be allowed.

Rejection under 35 U.S.C. §103:

Claims 3, 9, 14, 17, 21 and 31 stand rejected under 35 U.S.C. 35 U.S.C. §103(a) over Yamada in view of Applicant's admitted prior art. Applicant respectfully submits that claims 3, 9, 14, 17, 21 and 31 are not unpatentable over Yamada and requests reconsideration.

The Office Action states (p. 4, item 5) that "Yamada et al. did not clearly disclose a method as recited in claim 1, wherein individual address extensions identify address ranges associated with one or more peripheral devices." As such, the Examiner has admitted, on the record, that Yamada does not anticipate the subject matter recited in claim 1, and fails to provide the affirmatively-recited aspects of the claimed subject matter. The Office Action further states that "Nevertheless, this feature is shown by the applicants' admitted prior art, where each device is assigned with an address range (specification page 2, lines 1 - 3, page 3, lines 6 -21)."

Yamada is silent with respect to addressing of peripheral devices. In fact, Yamada is void of the term "peripheral". Yamada teaches (col. 7, line 29 et seq.) that:

In the embodiment shown in FIG. 3A, the page entry field selection unit 320 receives all of the bits of the virtual address except the bits of the offset field for the smallest page size supported by the embodiment. Since the smallest page size supported by the embodiment is a 4K page size that requires bits 11:0 of the virtual address as the offset field, the page entry field selection unit 320 receives all the bits of the virtual address except bits 11:0. However, alternative embodiments may provide any number of different bits from the virtual address to the page entry field selection unit 320, including: 1) all of the bits of the virtual address; 2) not all of the most significant bits; etc.

Each of the translation unit 300, the page entry field selection unit 320, the page table entry address generator 325, and the page size storage area 315 may be implemented in hardware and/or

software. In typical computer systems, the page table 310 is stored in main memory. In one embodiment of the invention, the translation unit 300, the page entry field selection unit 320, the page table entry address generator 325, and the page size storage area 315 are implemented in hardware on a processor, while the execution of the operating system on that processor creates and maintains the page table 310 in main memory.

As such, Yamada teaches addressing schemata appropriate to main memory units. The teachings of Yamada are rendered unsuitable for their intended purpose in adapting the teachings of Yamada to attempt to arrive at the subject matter of any of Applicant's claims encompassing peripheral device addressing. It is improper to employ a reference in a manner that renders the teachings of the reference unsuitable for their intended purpose, as is explained below in more detail with reference to MPEP §2143.01 entitled "Suggestion or Motivation To Modify the References". This MPEP section states, in a subsection entitled "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE", that "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)".

Additionally, the Office Action states that "it would have been obvious" to modify the teachings of Yamada. However, this unsupported conclusion does not reflect the test for unpatentability.

With respect to all such allegations, as there is no basis for the Examiner's contentions within the cited reference, the only possible motivation for these contentions is hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for modifying the cited reference.

The Examiner is reminded that hindsight reconstruction is not an appropriate basis for a §103 rejection. (See, e.g., *Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) (explaining that hindsight reconstruction is an improper basis for rejection of a claim).) Such an ad hoc conclusion also fails to provide evidence of motivation or suggestion to modify (see *In re Dembicza*, *infra*).

Further, there is no basis for the Examiner's contentions within the cited reference. No motivation is identified in the reference for the proposed modification and additions to the disclosure of the reference. Moreover, no evidence to motivate modification of the reference is identified. Against this backdrop, the rejection clearly employs an improper 'obvious to try' standard for finding unpatentability (discussed *infra*).

Applicant notes the requirements of MPEP §2143, entitled "Basic Requirements of a Prima Facie Case of Obviousness" (see also MPEP §706.02(j), entitled "Contents of a 35 U.S.C. 103 Rejection."). MPEP §2143 states that "To establish a prima facie case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." Inasmuch as the reference fails to teach or disclose the elements recited in the claims, the reference cannot provide motivation to modify their teachings to arrive at the invention as claimed, and the Examiner has identified no such teaching or disclosure in the reference. As a result, the first prong of the test cannot be met.

MPEP §2143 further states that "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Inasmuch as the reference fails to provide all of the features recited in Applicant's claims, the third prong of the test is not met. As a result, there cannot be a reasonable expectation of success. As such, the second prong of the test cannot be met.

MPEP §2143 additionally states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." This fourth criterion cannot be met because the reference fails to teach or disclose the elements recited in the claim.

In fact, Yamada is directed solely to a virtual addressing scheme for memory accession. The claimed subject matter addresses a broader range of issues including accession of peripheral devices. There is no motivation or suggestion in Yamada to even consider the problems addressed by the instant disclosure, and no guidance whatsoever to point the artisan towards the claimed subject matter.

Accordingly, the unpatentability rejections fail all of the criteria for establishing a *prima facie* case of obviousness as set forth in the MPEP.

Further, suggestion to modify as put forth in the Office Action appears to employ an improper "obvious to try" rationale, as is discussed below in more detail with reference to MPEP §2145(X)(B). This MPEP section states that:

The admonition that 'obvious to try' is not the standard under §103 has been directed mainly at two kinds of error. In some cases, what

would have been 'obvious to try' would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful.... In others, what was 'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it. *In re O'Farrell*, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted).

No guidance has been identified within the reference to determine which elements to pick or choose from the reference, or of how to couple them to somehow arrive at subject matter such as is claimed.

Moreover, with respect to all of the unpatentability rejections, no evidence has been provided as to why it would be obvious to modify the teachings of the reference. Evidence of a suggestion to combine or modify may flow (i) from the prior art reference itself, (ii) from the knowledge of one skilled in the art or (iii) from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembicza*k, 175 F.3d 994, 998 (Fed. Cir. 1999).

For at least these reasons, Applicant respectfully requests that the §103 rejections be withdrawn, and that Applicant's claims 3, 9, 14, 17, 21 and 31 be allowed.

Conclusion

Claims 1-36 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this

case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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By: 
Frederick M. Fliegel
Reg. No. 36,138
(509) 324-9256 x239

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